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LAW OFFICES
SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
WASHINGTON, DC 20037-3213
TELEPHONE (202) 293-7060
FACSIMILE (202) 293-7860
www.sughrue.com

October 24, 2000

BOX PCT

Assistant Commissioner for Patents
Washington, D.C. 20231

PCT/JP99/05693
-filed October 15, 1999

Re: Application of Atsushi ITO, Yasuji HIRAMATSU,
Yasutaka ITO, and Masakazu FURUKAWA
WAFER PROBER
Our Ref: Q60755

Dear Sir:

The following documents and fees are submitted herewith in connection with the above application for the purpose of entering the National stage under 35 U.S.C. § 371 and in accordance with Chapter II of the Patent Cooperation Treaty:

- ☒ an English translation of the International Application.
- ☒ 9 sheets of drawings.
- ☒ an English translation of Article 34 amendments.
- ☒ a Preliminary Amendment.

The Declaration and Power of Attorney and Assignment will be submitted at a later date.

The Government filing fee is calculated, after entry of the attached Preliminary Amendment, as follows:

Total claims	20	-	20	=		x	\$18.00	=	\$0.00
Independent claims	4	-	3	=	1	x	\$78.00	=	\$78.00
Base Fee									\$840.00
TOTAL FEE									\$918.00

A check for the statutory filing fee of **\$918.00** is attached. You are also directed and authorized to charge or credit any difference or overpayment to said Account. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16, 1.17 and 1.492

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SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC

Assistant Commissioner for Patents
U.S. Application based on International Appln. No. PCT/JP99/05693

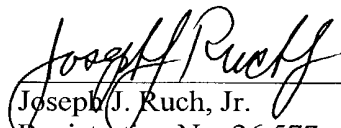
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which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from October 15, 1999, based on International Application No. PCT/JP99/05693.

Respectfully submitted,

SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860



Joseph J. Ruch, Jr.
Registration No. 26,577

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Atsushi ITO, Yasuji HIRAMATSU,
Yasutaka ITO, and Masakazu FURUKAWA

Appln. No.: (Not Yet Designated)

Group Art Unit: Unknown

Filed: October 24, 2000

Examiner: Unknown

For: WAFER PROBER

October 24, 2000

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Prior to examination of the above-identified application,
please amend the application as follows:

IN THE CLAIMS:

In claim 3, at line 1, delete "or 2".

5. (twice amended) A wafer prober according to claim 1
[which comprises a ceramic substrate and a conductor layer formed
on the surface thereof], wherein said ceramic substrate is
equipped with a Peltier device.

6. (twice amended) A wafer prober according to claim 1
[which comprises a ceramic substrate and a conductor layer formed
on the surface thereof], wherein on said ceramic substrate
channels are formed.

Appln. No.: (Not Yet Designated)
Atsushi ITO et al

8. (twice amended) The wafer prober according to claim 1 [which comprises a ceramic substrate and a conductor layer formed on the surface thereof], wherein said conductor layer is composed of porous material.

Please add the following claims.

--9. The wafer prober according to claim 2, wherein said ceramic substrate is equipped with a temperature control means.

10. The wafer prober according to claim 9, wherein said temperature control means is a heating element.

11. A ceramic substrate for a wafer prober which has a conductor layer formed on the surface thereof, wherein said ceramic substrate is composed of at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

12. A ceramic substrate for a wafer prober which has a conductor layer formed on the surface thereof, wherein in said ceramic substrate at least one conductor layer is formed.

13. The ceramic substrate for a wafer prober according to claim 11, wherein said ceramic substrate is equipped with a temperature control means.

PRELIMINARY AMENDMENT

Appln. No.: (Not Yet Designated)
Atsushi ITO et al

14. The ceramic substrate for a wafer prober according to claim 12, wherein said ceramic substrate is equipped with a temperature control means.

15. The ceramic substrate for a wafer prober according to claim 13, wherein said temperature control means is a heating element.

16. The ceramic substrate for a wafer prober according to claim 14, wherein said temperature control means is a heating element.

17. A ceramic substrate according to claim 11, wherein said ceramic substrate is equipped with a Peliter device.

18. A ceramic substrate according to claim 11, wherein on said ceramic substrate channels are formed.

19. The ceramic substrate for a wafer prober according to claim 14, wherein said channels formed on the surface of said ceramic substrate are provided with air suction holes.

20. A ceramic substrate according to claim 11, wherein said conductor layer is composed of porous material.--

PRELIMINARY AMENDMENT

Appln. No.: (Not Yet Designated)

Atsushi ITO et al

REMARKS

Claims 3, 5, 6, and 8 have been amended and claims 9-20 have been added hereinabove to place the claims in desired appropriate form for examination. Thus all of the claims are now in appropriate form, and the Examiner is respectfully requested to proceed with the examination.

Early favorable action is earnestly solicited.

In the event that the Examiner believes that it may facilitate the further prosecution of this application, the Examiner is invited to contact the undersigned attorney at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,

SUGHRUE, MION, ZINN,
MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3202
(202) 293-7060



Joseph J. Ruch, Jr.
Registration No. 26,577

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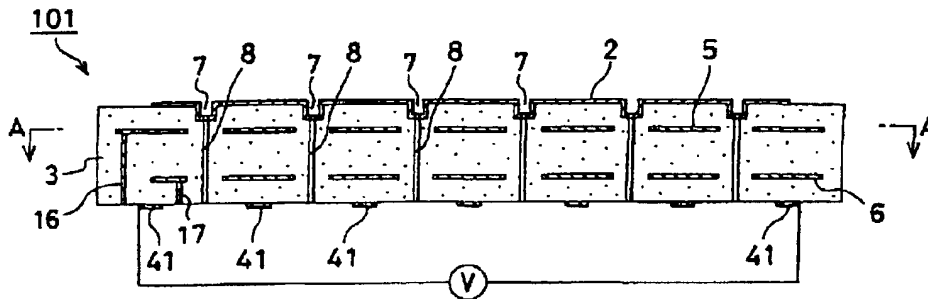
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- (74) 代理人: 安富康男, 外 (YASUTOMI, Yasuo et al.); 〒532-0011 大阪府大阪市淀川区西中島5丁目4番20号 中央ビル Osaka (JP).
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- (71) 出願人 (米国を除く全ての指定国について): イビデン株式会社 (IBIDEN CO., LTD.) [JP/JP]; 〒503-0917 岐阜県大垣市神田町2丁目1番地 Gifu (JP).
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- (72) 発明者; および
(75) 発明者/出願人 (米国についてのみ): 伊藤 淳 (ITO, Atsushi) [JP/JP], 平松 靖二 (HIRAMATSU, Yasuji)
- 2文字コード及び他の略語については、定期発行される各PCTガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(54) Title: WAFER PROBER

(54) 発明の名称: ウエハプローバ



(57) Abstract: A lightweight wafer prober of good temperature characteristic, which is unlikely to warp when its probe card is pressed, thereby effectively preventing damage to silicon wafers and measurement errors. The wafer prober includes a conductor layer formed on the surface of a ceramic substrate.

/ 続葉有 /

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(57) 要約:

本発明は、軽量で昇温、降温特性に優れており、しかも、プローブカードを押圧した場合にも反りがなく、シリコンウエハの破損や測定ミスを有効に防止することができるウエハプローバを提供することにある。

本発明は、セラミック基板の表面に導体層が形成されてなることを特徴とするウエハプローバである。

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SPECIFICATION

WAFER PROBER

5. TECHNICAL FIELD

The present invention relates to a wafer prober for use chiefly in semiconductor industry, and more particularly a wafer prober which is thin and lightweight and has a good thermal response kinetics.

10

BACKGROUND ART

The semiconductor is a product of great importance to various industries and the semiconductor chip is manufactured by, for example, slicing a silicon single crystal to a predetermined thickness to prepare a silicon wafer and constructing various circuits on the wafer.

The process for producing such a semiconductor chip must include a probing step for checking, in the silicon wafer stage, whether various electrical characteristics will be materialized as designed and the so-called prober is used for this purpose.

As such probers, Japanese Patent Publication 2587289, Japanese Kokoku Publication Hei-3-40947 and Japanese Kokai Publication Hei-11-31724, among others, describe wafer probers each equipped with a metallic chuck top comprising aluminum alloy, stainless steel or the like [Fig. 13].

With such a wafer prober, as illustrated in Fig. 12, for instance, silicon wafer W is set on the wafer prober 501, the probe card 601 having tester pins is pressed against the silicon wafer W, and then an electric voltage is applied under heating and cooling to perform a conductivity test.

However, any wafer prober equipped with such a metallic chuck top was found to have the following drawbacks.

In the first place, because it comprises a metal, the chuck top is, of necessity, as thick as approximately 15 mm. Such a thickness is needed for chuck top because if it is formed with

a thin metal sheet, the chuck top will warp or be strained as it is pressed by the tester pins of the prober card, with the result that the silicon wafer disposed on the metal sheet tends to be damaged or tipped.

5 Therefore, the chuck top must be sufficiently increased in thickness but doing so results in increased weight and bulk.

Moreover, despite the use of a metal having a high thermal conductivity, the thermal response kinetics are poor, that is to say the temperature of the chuck top sheet does not quickly
10 follow the change in voltage or current so that the temperature can hardly be controlled and, when a silicon wafer is set thereon at a high temperature, is quite uncontrollable.

SUMMARY OF THE INVENTION

15 In the light of the above state of the art, the present invention has for its object to provide a wafer prober which is lightweight, excellent in thermal response kinetics and free from warpage upon pressing with a probe card, thus capable of effective protecting itself against damage to the silicon wafer
20 and measurement error.

To accomplish the above object, the inventors of the present invention made intensive investigations and found that when a high-rigidity ceramic material is provided with a conductor layer for use as a chuck top conductor layer in lieu
25 of a metallic chuck top, there is obtained a wafer prober which is thin and yet free from the trouble of warpage.

Furthermore, the inventors discovered that the poor thermal response characteristic of the wafer prober having a metallic chuck top despite the use of a metal of high thermal
30 conductivity is because the thickness of the metal sheet is too great as a result that the sheet has high heat capacity and the inventors arrived at the novel technical concept, which is diametrically opposite to the common belief, that even though its thermal conductivity is inferior to metal, the use of a ceramic
35 material is conducive to decrease in heat capacity by reducing

the thickness of it, thus realizing improvements in thermal response kinetics. The present invention has come forth from the above finding.

The present invention, therefore, is directed to a wafer
5 prober which comprises a ceramic substrate and a conductor layer
 (chuck top conductor layer) formed on the surface thereof.

In said wafer prober, said ceramic substrate is preferably equipped with a temperature control means.

In said wafer prober, said ceramic substrate is preferably
10 composed of at least one member selected from the group
 essentially consisting of nitride ceramics, carbide ceramics
 and oxide ceramics.

Moreover, said temperature control means is preferably a Peltier device or a heating element.

15 Further, in said wafer prober, said ceramic substrate
 preferably has at least one or more conductor layers therein,
 with its surface preferably being formed with channels.

Furthermore, the channels provided with air suction holes are preferably formed on the surface of said ceramic substrate.

20

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-section view showing an example of the wafer prober according to the present invention.

Fig. 2 is a plan view of the wafer prober shown in Fig.
25 1.

Fig. 3 is a bottom view of the wafer prober shown in Fig.
1.

Fig. 4 is a sectional elevation view taken along the line A-A of Fig. 1.

30 Fig. 5 is a schematic cross-section view showing another
 example of the wafer prober according to the present invention.

Fig. 6 is a schematic cross-section view showing still another example of the wafer prober according to the present invention.

35 Fig. 7 is a schematic cross-section view showing another

example of the wafer prober according to the present invention.

Fig. 8 is a schematic cross-section view showing the wafer prober of the present invention as assembled with a platform.

Fig. 9 (a) is a schematic longitudinal section view of
 5 the wafer prober of the present invention as assembled with
 another platform and Fig. 9 (b) is a sectional view taken along
 the line B-B of (a).

Fig. 10 (a) to (d) are schematic cross-section views
 illustrating several stages of the process for manufacturing
 10 the wafer prober according to the present invention.

Fig. 11 (e) to (g) are schematic cross-section views
 illustrating several stages of the process for manufacturing
 the wafer prober according to the present invention.

Fig. 12 are schematic cross-section views illustrating
 15 the conductivity test performed with the wafer prober of the
 present invention.

Fig. 13 is a schematic cross-section view illustrating
 a conventional wafer prober.

20 EXPLANATION OF THE NUMERIC SYMBOLS

- 101, 201, 301, 401 wafer prober
- 2 chuck top conductor layer
- 3 ceramic substrate
- 5 guard electrode
- 25 6 ground electrode
- 7 channel
- 8 suction hole
- 10 heat insulator
- 11 platform
- 30 12 blow-out nozzle
- 13 suction port
- 14 cooling medium injection port
- 15 prop
- 16, 17 through hole
- 35 180 blind holes

19, 190, 191 external terminal pin
41, 42 heating element
410 protective layer
43 metal wire
5 44 Peltier device
440 thermoelectronic element
441 ceramic substrate
51 conductive layer
52 non-conductor layer-forming areas

10

DETAILED DESCRIPTION OF THE INVENTION

The present invention is now described in detail.

The wafer prober of the present invention comprises a ceramic substrate and a conductor layer (chuck top conductor layer) on the surface thereof. This conductor layer will
15 hereinafter be referred to as "chuck top conductor layer".

Since a high-rigidity ceramic substrate is used in the present invention, the chuck top does not undergo warpage when pressed by the tester pins of a probe card so that the thickness
20 of said chuck top may be smaller than the metallic chuck top.

Furthermore, because the thickness of said chuck top can thus be reduced in comparison with a metallic chuck top, the thermal response kinetics of the wafer prober can be improved as the heat capacity is decreased despite the comparatively low
25 thermal conductivity of ceramics as compared with metals.

Fig. 1 is a schematic cross-section view showing one example of the wafer prober of the present invention; Fig. 2 is a plan view thereof; Fig. 3 is a bottom view thereof; and Fig. 4 is a sectional view taken along the line A-A of Fig. 1.

30 This wafer prober comprises a ceramic substrate 3 which is circular in plan view and has a plurality of concentric channels 7 formed on its surface, and a plurality of suction holes 8 for attracting a silicon wafer by suction as formed strategically in a part of said channels 7 and a chuck top conductor layer
35 2 formed in a circular fashion for connection to electrodes of

a silicon wafer as covering most of said ceramic substrate 3 inclusive of said channels 7.

On the other hand, the bottom surface of the ceramic substrate 3 is provided, as shown in Fig. 3, with a plurality of coils of a heating element 41 in a concentric array in plan view for controlling the temperature of the silicon wafer, with both ends of said coils of heating element 41 being secured to an external terminal pin 191. In addition, a guard electrode 5 and a ground electrode 6 are disposed in said ceramic substrate 3 for avoiding stray capacitance and noise.

The wafer prober of the present invention may assume, for example, the structures illustrated in Figs. 1 to 4. In the following, each component of said wafer prober and other examples of the wafer prober of the present invention will be described serially in detail.

The ceramic substrate for use in the wafer prober of the present invention is preferably at least one member selected from the group essentially consisting of nitride ceramics, carbide ceramics and oxide ceramics.

The nitride ceramics mentioned above includes metal nitride ceramics such as aluminum nitride, silicon nitride, boron nitride and titanium nitride ceramics, among others.

The carbide ceramics mentioned above includes metal carbide ceramics such as silicon carbide, zirconium carbide, titanium carbide, tantalum carbide and tungsten carbide ceramics, among others.

The oxide ceramics mentioned above includes metal oxide ceramics such as alumina, zirconia, cordierite and mullite ceramics, among others.

Those ceramics can be used each independently or in combination.

Among these ceramics, nitride ceramics and carbide ceramics are preferred to oxide ceramics because the former ceramics are superior in thermal conductivity.

Moreover, among nitride ceramics, aluminum nitride

ceramics is the best choice because it has the highest thermal conductivity of $180 \text{ W/m}\cdot\text{K}$.

The ceramics mentioned above preferably contain 200 to 1000 ppm of carbon. This is partly because the electrode pattern of the ceramic substrate can be hidden and partly because a high radiant heat can be obtained. The carbon may be a crystalline carbon which can be detected by X-ray diffraction analysis or an amorphous carbon which cannot be so detected.

10 The thickness of the ceramic substrate of the chuck top
of the present invention should be greater than the thickness
of the chuck top conductor layer and, to be concrete, is preferably
within the range of 1 to 10 mm.

Since the reverse side of the silicon wafer is utilized as the electrode in the present invention, the ceramic substrate is formed with a chuck top conductor layer on its surface.

The thickness of said chuck top conductor layer is preferably 1 to 20 μm . If the conductor layer is less than 1 μm in thickness, its resistance will be too high as a result that the layer cannot function as an electrode. On the other hand, if the thickness exceeds 20 μm , the layer will be liable to peel off due to the stress of the conductor.

The chuck top conductor layer can be constructed using at least one kind of metal selected from among high-melting metals such as copper, titanium, chromium, nickel, noble metals (e.g. 25 gold, silver and platinum), tungsten and molybdenum.

The chuck top conductor layer may be a porous layer of metal or conductive ceramics. In the case of a porous layer, it is unnecessary to provide channels for attraction by suction as will be described later, so that the destruction of the wafer owing to the presence of such channels can be precluded and a uniform attraction by suction over the entire surface can be realized.

As such a porous material, a sintered metal can be used.

The porous material can be used in a thickness of 1 to
35 200 μm . The porous material can be secured to the ceramic

substrate by soldering or brazing.

The chuck top conductor layer preferably contains nickel. This is because such a layer is so hard that it is not easily deformed by the pressing force of the tester pins.

5 A specific example of the chuck top conductor layer is a conductor layer constructed by sputtering nickel and then forming an electroless plated nickel layer thereon or a conductor layer constructed by sputtering titanium, molybdenum and nickel in that order and further depositing nickel in superimposition
10 by electroless plating or electroplating.

The conductor layer may also be a layer constructed by sputtering titanium, molybdenum and nickel in that order and further depositing copper and nickel serially, both by electroless plating. The formation of a copper layer
15 contributes to a reduced resistance value of the chuck top electrode.

A further alternative conductor layer may be a conductor layer formed by sputtering titanium and copper in that order and further depositing nickel thereon by electroless plating
20 or electroplating.

Furthermore, it is possible to construct a conductor layer by sputtering chromium and copper in that order and then depositing nickel in superimposition by electroless plating or electroplating.

25 Titanium and chromium, mentioned above, contribute to improved adhesion of the conductor layer to ceramics, while molybdenum insures better adhesion to nickel.

The preferred thickness of titanium and chromium layers is 0.1 to 0.5 μm , that of molybdenum is 0.5 to 7.0 μm , and that
30 of nickel is 0.4 to 2.5 μm .

Said chuck top conductor layer is preferably formed with a noble metal layer (gold, silver, platinum or palladium) on its surface, because the noble metal layer prevents contamination due to migration of base metals. The preferred thickness of
35 said noble metal layer is 0.01 to 15 μm .

of the metal powder and the nitride or carbide ceramics are sintered together via the metal oxide to be unified so that good adhesion between the metal powder and the nitride or carbide ceramics can be insured.

5 The metal oxide mentioned above is preferably at least one member selected from the group consisting of lead oxide, zinc oxide, silica, boron oxide (B_2O_3), alumina, yttria and titania. The reason for use of metal oxide is that those oxides improve the adhesion between the metal powder and the nitride
10 or carbide ceramics without increasing the resistance value of the heating element.

 The proportion of the metal oxide mentioned above is preferably not less than 0.1 weight % and less than 10 weight % based on the metal powder. Within this range, the adhesion
15 between the metal powder and the nitride or carbide ceramics can be improved without causing too much increase in resistance.

 The preferred proportions of lead oxide, zinc oxide, silica, boron oxide (B_2O_3), alumina, yttria and titania, with the total amount of metal oxide being taken as 100 weight parts, are that
20 lead oxide accounts for 1 to 10 weight parts, silica for 1 to 30 weight parts, boron oxide for 5 to 50 weight parts, zinc oxide for 20 to 70 weight parts, alumina for 1 to 10 weight parts, yttria for 1 to 50 weight parts and titania for 1 to 50 weight parts. However, it is preferred that the total of them does
25 not exceed 100 weight parts. That is because those ranges are particularly useful for improving adhesion to nitride ceramics.

 When the heating element is disposed on the surface of the ceramic substrate, the surface of the heating element is preferably covered with a metal layer 410 [Fig. 11(e)]. The
30 heating element comprises a sintered body of metal powder and, if exposed, is liable to be oxidized to cause changes in resistance value. This oxidation can be prevented by covering the surface of the heating element with a metal layer.

 The thickness of the metal layer is preferably 0.1 to 10
35 μm . Within this range, the oxidation of the heating element

can be precluded without alteration in the resistance value of the heating element.

The metal for use in said coating may be any non-oxidizable metal. More particularly, at least one metal selected from the group consisting of gold, silver, palladium, platinum and nickel can be used with advantage. Among them, nickel is particularly preferred. This is because while the heating element must be provided with terminals for connection to a power source and those terminals are soldered to the heating element, nickel prevents thermal diffusion of the solder. As connection terminals, terminal pins comprising copal can be used.

When the heating element is formed within the heater plate, the surface of the heating element is not oxidized so that it need not be covered. When the heating element is thus formed within the heater plate, the surface of the heating element may be partially exposed.

As the metal foil for use as the heating element, a heating element formed by pattern-etching a nickel foil or a stainless steel foil is preferred.

The patterned metal foil may be bonded with resin film or the like.

As the metal wire, there can be mentioned tungsten wire, molybdenum wire and the like.

The use of a Peltier device as said temperature control means is advantageous in that both heating and cooling can be effected by changing the direction of flow of an electric current.

As illustrated in Fig. 7, a Peltier device is formed by connecting p and n type thermoelectric elements 440 in series and bonding them to a ceramic board 441, for instance.

As the Peltier device, there can be mentioned a silicon-germanium device, a bismuth-antimony device, and a lead-tellurium device.

In the present invention, at least one electrically conductive layer is preferably interposed between the temperature control means and the chuck top conductor layer.

The guard electrode 5 and ground electrode 6 shown in Fig. 1 correspond to said conductor layers.

The guard electrode 5 is an electrode for canceling the stray capacitance in the measuring circuit and is given the earth potential of the measuring circuit (i.e. the chuck top conductor layer 2 in Fig. 1). The ground electrode 6 is provided for canceling the noise from the temperature control means.

The preferred thickness of these electrode is 1 to 20 μ m. If the electrodes are too thin, the resistance value is increased. If they are too thick, the ceramic substrate may undergo warpage or the thermal shock resistance will be decreased.

Each of said guard electrode 5 and ground electrode 6 is preferably disposed in the form of a grid as shown in Fig. 4. Thus, a multiplicity of orthogonal non-conductor layer-forming areas 52 are laid out regularly in a circular conductor layer 51. This arrangement is used for improving the adhesion between the ceramics on and underneath the conductor layer.

The surface of the chuck top layer of the wafer prober according to the present invention is preferably provided with channels 7 and air suction holes 8 as illustrated in Fig. 2. A plurality of suction holes 8 are arranged to insure a uniform suction force. By this means, after placement of a silicon wafer W, the air can be aspirated from the suction holes 8 to attract the silicon wafer W.

The wafer prober according to the present invention includes, for example, a wafer prober 101 which, as shown in Fig. 1, comprises a ceramic substrate 3, a heating element 41 disposed on the bottom side thereof, a chuck top conductor layer 2, and a guard electrode 5 layer and a ground electrode 6 layer interposed between the heating element 41 and chuck top conductor layer 2; a wafer prober 201 which, as shown in Fig. 5, comprises a ceramic substrate 3, a flat heating element 42 disposed within said ceramic substrate 3, a chuck top conductor layer 2, and a guard electrode 5 and a ground electrode 6 interposed between

Fig. 9 (a) is a schematic longitudinal section view of another platform and (b) is a sectional view taken along the line B-B of (a). As shown in Fig. 9, this platform is provided with a plurality of props 15 for preventing warpage of the wafer prober upon being pressed by the tester pins of the probe card.

The platform may comprise aluminum alloy or stainless steel.

A typical process for manufacturing the wafer prober of the present invention is now described, reference being had to the sectional views in Figs. 10 and 11.

(1) First, a powder of ceramic material such as oxide ceramics, nitride ceramics and carbide ceramics is admixed and molded with a binder and a solvent to prepare a green sheet 30.

As the ceramic powder mentioned above, a powder of aluminum nitride or silicon carbide, for instance, can be used. Where necessary, a sintering aid such as yttria can be added.

The binder mentioned above is preferably at least one member selected from the group consisting of acrylic binder, ethylcellulose, butylcellosolve and polyvinyl alcohol.

As the solvent, it is preferable to use at least one member selected from the group consisting of α -terpineol and glycol.

The paste obtained by admixing the above materials is molded into a sheet by the doctor blade method to fabricate said green sheet 30.

Where necessary, this green sheet 30 may be provided with through-holes for accepting the silicon pins of the wafer support and cavities for embedding thermocouples. The through-holes and cavities can be formed by punching, for instance.

The preferred thickness of the green sheet 30 is about 0.1 to 5 mm.

Then, the green sheet 30 is printed with the guard electrode and ground electrode.

In consideration of the rate of shrinkage of the green sheet 30, this printing is performed so as to insure a predetermined aspect ratio to thereby provide a guard electrode

Those prints can be provided by using a conductive paste containing a conductive ceramic or metal powder.

As said metal powder, a powder of, for example, tungsten, molybdenum, platinum, or nickel can be used.

The optimum paste is a compounded mixture of 85 to 97 weight parts of a metal powder or a conductive ceramic powder, 1.5 to 10 weight parts of at least one kind of binder selected from among acrylic binder, ethylcellulose, butylcellosolve and polyvinyl alcohol, and 1.5 to 10 weight parts of at least one kind of solvent selected from among α -terpineol, glycol, ethanol and butanol.

Then, as shown in Fig. 10 (a), the green sheet 30 provided with prints 50, 60, 160 and 170 is laminated with a green sheet 30 not provided with such prints. The unprinted green sheet 30 is laminated to the heating element side because the end faces of the plated-through holes will not be exposed and, hence, not oxidized in the sintering procedure for the formation of a heating element. If the sintering operation for the formation of a heating element is to be performed with the end faces of plated-through holes in the exposed state, it will be necessary to sputter a hardly oxidizable metal such as nickel. More preferably, a brazed gold of Au-Ni can be covered.

35 (2) Then, as shown in Fig. 10 (b), the laminate is hot-pressed

to sinter the green sheet and conductive paste.

The preferred sintering temperature is 1000 to 2000°C and the preferred sintering pressure is 100 to 200 kg/cm². This application of heat and pressure is carried out in an inert gas atmosphere. The inert gas that can be used for this purpose includes argon gas and nitrogen gas, among others. By the above procedure, plated-through holes 16 and 17, guard electrodes 5 and ground electrodes 6 are constructed.

(3) Then, as shown in Fig. 10 (c), channels 7 is formed on the surface of the sintered compact. The channels 7 are formed by means of a drill or by sand blasting, for instance.

(4) Then, as shown in Fig. 10 (d), the conductive paste is printed on the bottom side of the sintered compact and fired to construct a heating element 41.

(5) Then, as shown in Fig. 11 (e), the surface on which the silicon wafer is to be set (the surface formed with channels) is sputtered with titanium, molybdenum, nickel or the like, followed by deposition of nickel by electroless plating to complete a chuck top conductor layer 2. Simultaneously with the latter operation, a protective layer 410 is formed on the surface of the heating element 41, too, by nickel electroless plating.

(6) Then, as shown in Fig. 11 (f), suction holes 8 extending from the channels 7 to the reverse side and blind holes 180 for connection to external terminals are provided.

The internal wall of the blind hole is preferably rendered conductive at least in part and the conductive internal wall is preferably connected to the guard electrode, the ground electrode or the like.

(7) Finally, as shown in Fig. 11 (g), a solder paste is printed on the connective regions of the surface of the heating element 41 and with external pins 191 set in position, heated for reflow. The preferred heating temperature is 200 to 500°C.

The external terminals 19 and 190 are also equipped for the blind holes 180 via brazed gold. Where necessary, bottomed

holes can be formed and thermocouples be embedded therein.

The solder which can be used includes silver-lead, lead-tin, bismuth-tin and other alloy solders. The thickness of the solder layer is preferably 0.1 to 50 μm . Within this thickness range, an effective solder joint can be established.

While the wafer prober 101 [Fig. 1] was referred to as the objective product in the above description, said heating element can be printed on the green sheet to provide a wafer prober 201 [Fig. 5]. For the manufacture of the wafer prober 301 [Fig. 6], metal sheets to serve as said guard electrode and ground electrode and a metal wire to serve as said heating element may be embedded in a ceramic powder and the powder be sintered.

For the manufacture of the wafer prober 401 [Fig. 7], a Peltier device may be attached via a thermal-sprayed metal layer.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is now described in further detail.

Example 1

20 Production of wafer prober 101 [Fig. 1]

(1) A composition comprising 100 weight parts of aluminum nitride powder (Tokuyama Co., mean particle diameter; 1.1 μm), 4 weight parts of yttria (mean particle diameter; 0.4 μm), 11.5 weight parts of acrylic binder, 0.5 weight part of dispersant and 53 weight parts of alcohol (1-butanol and ethanol) was molded by the doctor blade method to provide a 0.47 mm-thick green sheet.

(2) After this green sheet was dried at 80°C for 5 hours, through holes for the plated-through holes for connecting the heating element to external terminal pins were pierced by punching.

(3) A conductive paste A was prepared by mixing 100 weight parts of a tungsten carbide powder having a mean particle diameter of 1 μm , 3.0 weight parts of acrylic binder, 3.5 weight parts of the solvent α -terpineol and 0.3 weight part of dispersant.

35 A conductive paste B was also prepared by mixing 100 weight

parts of a tungsten powder having a mean particle diameter of $3\text{ }\mu\text{m}$, 1.9 weight parts of acrylic binder, 3.7 weight parts of the solvent α -terpineol and 0.2 weight part of dispersant.

Then, a guard electrode grid pattern print 50 and a ground electrode grid pattern print 60 were formed on the green sheet by screen printing with the above conductive paste A.

In addition, the through holes for said plated-through holes for connection to terminal pins were filled with the above conductive paste B.

Then, 50 printed and unprinted green sheets were alternately laid up and bonded together at 130°C and 80 kg/cm^2 to provide a laminate [Fig. 10 (a)].

(4) This laminate was then degreased in nitrogen gas at 600°C for 5 hours and, then, hot-pressed at 1890°C and 150 kg/cm^2 for 3 hours to provide a 4 mm-thick aluminum nitride plate. From this plate, a disk with a diameter of 230 mm was cut out to provide a ceramic plate [Fig. 10 (b)]. The sizes of each plated-through hole 16 and 17 were 3.0 mm in diameter and 3.0 mm deep.

Each thickness of the guard electrode 5 and ground electrode 6 was $10\text{ }\mu\text{m}$, and the location of the guard electrode 5 was 1.2 mm away from the wafer-mounting surface and the location of the ground electrode 6 was 3.0 mm away from the wafer-mounting surface.

(5) The plate obtained in the above step (4) was polished with a diamond wheel, and with a mask set in position, blasting with SiC or the like was performed to provide the surface with cavities for accommodating thermocouples (not shown) and a plurality of channels 7 (0.5 mm wide x 0.5 mm deep) for attraction of a silicon wafer by suction [Fig. 10 (c)].

(6) Then, a heating element 41 was printed on the side opposite to the wafer-mounting side. This printing was carried out using a conductive paste. The conductive paste used here was Solbest PS603D from Tokuriki Chemical Research Institute, which is generally used for the formation of plated-through holes in printed circuit boards. This conductive paste was a silver/lead

5 The silver had a mean particle diameter of 4.5 μ m and
 was flaky.

The heating element comprising sintered silver was 5 μ m in thickness and 2.4 mm wide and had an area resistivity of 7.7 m Ω /□ [Fig. 10 (d)].

The thicknesses of the films formed were determined from the image outputs of a fluorescent X-ray analyzer. Thus, the thickness of the titanium layer was $0.3\text{ }\mu\text{m}$, that of the molybdenum layer was $2\text{ }\mu\text{m}$, and that of the nickel layer was $1\text{ }\mu\text{m}$.

(9) Using a nickel electroless plating bath comprising an aqueous solution of nickel sulfate (30 g/L), boric acid (30 g/L), ammonium chloride (30 g/L) and Rochelle salt (60 g/L) and a nickel electroplating bath comprising nickel sulfate (250 to 350 g/L), nickel chloride (40 to 70 g/L) and boric acid (30 to 50 g/L)

and adjusted to pH 2.4 to 4.5 with sulfuric acid, the ceramic board obtained in the above step (8) was immersed to deposit a 7 μ m-thick nickel layer with a boron content of not more than 1 weight % on the surface of said sputtered metal layer and the nickel layer so formed was annealed at 120°C for 3 hours.

The surface of the heating element did not allow a current flow and, therefore, was not covered with electroplated nickel.

Then, the board was immersed in a gold electroless plating solution containing potassium gold cyanide (2 g/L), ammonium chloride (75 g/L), sodium citrate (50 g/L) and sodium hypophosphite (10 g/L) at 93°C for 1 minute to form a 1 μ m-thick gold layer on the plated nickel layer 15 [Fig. 11 (e)].

(10) Air suction holes 8 extending from the channels 7 to the reverse side of the board were drilled and blind holes 180 for exposing the plated-through holes 16 and 17 were further provided [Fig. 10 (f)]. The blind holes 180 were filled with a brazed gold of Ni-Au alloy (Au: 81.5 wt. %, Ni: 18.4 wt. %, impurity: 0.1 wt. %), which was then heated and caused to reflow at 970°C for connection to external terminal pins 19 and 190 of copal [Fig. 11 (g)]. Moreover, the heating element was provided with external pins 191 comprising copal via a solder layer (tin:lead = 9:1).

(11) Then, a plurality of thermocouples for temperature control were embedded in the cavities to provide a finished wafer prober 101 equipped with a heater.

(12) This wafer prober 101 was assembled with a stainless steel platform having a sectional configuration shown in Fig. 8 through a heat insulator 10 comprising ceramic fiber (Ibiden, Ibiwool™). This platform 11 was equipped with cooling gas ejection nozzles 12 for regulating the temperature of the wafer prober 101. Moreover, it was equipped with a suction hole 13 for aspirating the air necessary to attract the silicon wafer.

Example 2

35 Production of wafer prober 201 [Fig. 5]

(4) This laminate was then degreased in nitrogen gas at 600°C for 5 hours and, then, hot-pressed at 1890°C and 150 kg/cm² for 3 hours to provide a 3 mm-thick aluminum nitride plate. From this plate, a disk with a diameter of 230 mm was cut out to provide a ceramic board. The sizes of each plated-through hole were 2.0 mm in diameter and 3.0 mm deep.

Each thickness of the guard electrode 5 and ground electrode 6 was 6 μm , and the location of the guard electrode 5 was 0.7 mm away from the wafer-mounting surface, the location of the ground electrode 6 was 1.4 mm away from the wafer-mounting surface, and the location of the heating element was 2.8 mm away from the wafer-mounting surface.

(5) The board obtained in the above step (4) was polished with a diamond wheel, and with a mask set in position, blasting with SiC or the like was performed to provide the surface with cavities for accommodating thermocouple (not shown) and a plurality of channels 7 (0.5 mm wide x 0.5 mm deep) for attraction of a silicon wafer by suction.

(6) The surface formed with channels 7 were serially sputtered to deposit a titanium layer, a molybdenum layer and a nickel layer. As the sputtering equipment, Japan Vacuum Technology's SV-4540 was used. The sputtering conditions were; gas pressure: 0.6 Pa, temperature: 100°C and power: 200 W. The sputtering time was adjusted for each metal species within the range of 30 seconds to 1 minute.

The thicknesses of the films thus obtained were determined from the image outputs of a fluorescent X-ray analyzer. Thus, the thickness of the titanium layer was 0.5 μm , that of the molybdenum layer was 4 μm , and that of the nickel layer was 1.5 μm .

(7) The ceramic board 3 obtained in the above step (6) was immersed in a nickel electroless plating bath comprising an aqueous solution of nickel sulfate (30 g/L), boric acid (30 g/L), ammonium chloride (30 g/L) and Rochelle salt (60 g/L) to deposit a 7 μm -thick nickel layer with a boron content of not more than 1 weight % on the surface of said sputtered metal layer and the nickel layer so formed was annealed at 120°C for 3 hours.

Then, the board was immersed in a gold electroless plating solution containing potassium gold cyanide (2 g/L), ammonium chloride (75 g/L), sodium citrate (50 g/L) and sodium

hypophosphite (10 g/L) at 93°C for 1 minute to form a 1 μm -thick

plated gold layer on the plated nickel layer.

(8) Air suction holes 8 extending from the channels 7 to the reverse side of the board were drilled and blind holes 180 for exposing the plated-through holes 16 and 17 were further provided.

5 The blind holes 180 were filled with a brazed gold of Ni-Au alloy (Au: 81.5 wt. %, Ni: 18.4 wt. %, impurity: 0.1 wt. %), which was then heated and caused to reflow at 970°C for connection to external terminal pins 19 and 190 comprising copal. The external terminals may comprise silicon wafer W.

10 (9) Then, a plurality of thermocouples for temperature control were embedded in the cavities to provide a wafer prober 201 equipped with a heater.

(10) This wafer prober 201 was assembled with a stainless steel platform having a sectional configuration shown in Fig. 9 through
15 a heat insulator 10 comprising ceramic fiber (Ibiden, Ibiwool™). This platform 11 was formed with props 15 for preventing warpage of the wafer prober. It was also equipped with a suction hole 13 for aspirating the air to attract the silicon wafer by suction.

20 Example 3

Production of wafer prober 301 [Fig. 6]

(1) A 10 μm-thick tungsten foil was punched to form a grid-like electrode.

Two sheets of the grid electrode (which were to serve as
25 a guard electrode 5 and a ground electrode 6, respectively) and a tungsten wire, as well as 100 weight parts of an aluminum nitride powder (Tokuyama Co., mean particle diameter: 1.1 μm) and 4 weight parts of yttria (mean particle diameter: 0.4 μm) were put in a mould and hot-pressed under nitrogen gas at 1890°C and
30 150 kg/cm² for 3 hours to prepare a 3 mm-thick aluminum nitride plate. From this plate, a disk with a diameter of 230 mm was cut out to provide a board.

(2) This board was caused to go through the steps (5) to (10) of Example 2 to provide a wafer prober 301 and this wafer prober
35 301 was set on the platform 11 of Fig. 8 as in Example 1.

Example 4

Manufacture of wafer prober 401 [Fig. 7]

After the steps (1) to (5) and (8) to (10) of Example 1
5 were repeated, nickel thermal spraying was carried out on the
surface opposite to the wafer-mounting surface. Then, a Peltier
device of lead-tellurium system was attached to provide a wafer
prober 401. As in Example 1, this wafer prober 401 was mounted
on the platform 11 shown in Fig. 8.

10

Example 5

Manufacture of a wafer prober using silicon carbide as the ceramic
substrate

Excepting the following particulars and conditions, the
15 procedure of Example 3 was otherwise repeated to manufacture
a wafer prober.

Thus, using 100 weight parts of a silicon carbide powder
having a mean particle diameter of $1.0\ \mu\text{m}$, two grid electrodes
(which were to serve as the guard electrode 5 and ground electrode
20 6, respectively) and a tungsten wire coated with a sol comprising
10 weight % of tetraethoxysilane, 0.5 weight % of hydrochloric
acid and 89.5 weight % of wafer, the sintering was performed
at the temperature of 1900°C . The sol mentioned above became
 SiO_2 on sintering to form an insulating layer.

25 Then, the wafer prober 301 thus obtained in Example 5 was
mounted on the platform 11 illustrated in Fig. 8 as in Example
1.

Example 6

30 Manufacture of a wafer prober using alumina as the ceramic
substrate

Except for the following particulars and conditions, the
procedure of Example 1 was otherwise repeated to manufacture
a wafer prober.

35 A composition prepared by mixing 100 weight parts of

alumina powder (Tokuyama Co., mean particle diameter 1.5μ m), 11.5 weight parts of acrylic binder, 0.5 weight part of dispersant and 53 weight parts of alcohol (1-butanol and ethanol) was molded by the doctor blade method to provide a 0.5 mm-thick green sheet. The sintering temperature was 1000°C .

The wafer prober thus obtained in Example 6 was mounted on the platform 11 shown in Fig. 8 as in Example 1.

Example 7

(1) A tungsten powder having a mean particle diameter of 3μ m was placed in a disk-shaped mould and hot-pressed under nitrogen gas at 1890°C and 150 kg/cm^2 for 3 hours to prepare a porous chuck top conductor layer of tungsten measuring 200 mm in diameter and 110μ m in thickness.

(2) Then, the steps (1) to (4) and (5) to (7) of Example 1 were repeated to provide a ceramic board equipped with the guard electrodes, ground electrodes and heating element.

(3) The porous chuck top conductor layer obtained in the above step (1) was mounted on the ceramic board through a brazed gold (same as the one used in the step (10) of Example 1) and heated for reflow at 970°C .

(4) The sequence of steps (10) to (12) of Example 1 was then repeated to provide a wafer prober.

The wafer prober obtained in this example uniformly attracted a semiconductor wafer to its chuck top conductor layer.

Comparative Example 1

Basically according to the method described in Japanese Kokoku Publication Hei-3-40947, a metallic wafer prober having the architecture shown in Fig. 12 was fabricated.

Thus, this wafer prober comprises a stainless steel disk measuring 230 mm in diameter and 15 mm in thickness, a mica layer 3B underneath said stainless steel disk and, as disposed further underneath said mica layer, a copper disk 100B measuring 230

mm in diameter and 20 mm in thickness. Further underneath the copper disk 100B, a Nichrome wire heating element 4B is attached via a mica layer 3B. The surface of the chuck top is formed with channels 7.

- 5 As in Example 1, the above wafer prober was mounted on the platform 11 illustrated in Fig. 8.

Comparative Example 2

- 10 Except that a 1.5 mm-thick stainless steel sheet was used as chuck top 1B and, underneath thereof, a mica layer 3B and a 1.5 mm copper sheet 100B were disposed in that order, a metallic wafer prober was fabricated according to otherwise the same manner as the wafer prober of Comparative Example 1.

- 15 This wafer prober was mounted on the platform 11 of Fig. 8 as in Example 1.

Evaluation method

- 20 On the wafer prober fabricated in each of the above examples and comparative examples, a silicon wafer W shown in Fig. 12 was set and a conductivity test was performed by pressing a probe card 601 under temperature control.

- 25 The time till the temperature had risen to 150°C was measured. In addition, the amount of warpage of the wafer prober upon being pressed by the probe card at a pressure of 15 kg/cm² was determined. The amount of warpage was measured with Kyocera form meter Nanoway™.

- 30 In the case of the wafer prober according to Example 2, it was first set on a platform equipped with anti-warpage props and measured for warpage and, then set on a prop-free platform shown in Fig. 8 and measured for warpage. The results are shown in Table 1.

Table 1

	Warpage (μ m)	Time (min.)
Example 1	1	3.0

Example 2	*1 0.5	2.9
	*2 1	2.8
Example 3	1.5	3.0
Example 4	1.5	3.0
Example 5	2.0	4.0
Example 6	3.0	7.0
Example 7	1	2.9
Compar. Ex. 1	1	15
Compar. Ex. 2	15	5

Note *1: With props

*2: Without props

INDUSTRIAL APPLICABILITY

5 As described above, the wafer prober of the present invention is not only light in weight and excellent in thermal response kinetics, but also free from warping upon pressing with a probe card, so that breakage of silicon wafers and measurement errors can be effectively prevented.

Amendment under Article 34

CLAIMS

- 5 1. (Amended) A wafer prober which comprises a ceramic substrate and a conductor layer formed on the surface thereof, wherein said ceramic substrate is composed of at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.
- 10 2. (Amended) A wafer prober which comprises a ceramic substrate and a conductor layer formed on the surface thereof, wherein in said ceramic substrate at least one conductor layer is formed.
- 15 3. The wafer prober according to Claim 1 or 2, wherein said ceramic substrate is equipped with a temperature control means.
- 20 4. (Amended) The wafer prober according to Claim 3, wherein said temperature control means is a heating element.
- 25 5. (Amended) A wafer prober which comprises a ceramic substrate and a conductor layer formed on the surface thereof, wherein said ceramic substrate is equipped with a Peltier device.
- 30 6. (Amended) A wafer prober which comprises a ceramic substrate and a conductor layer formed on the surface thereof, wherein on said ceramic substrate channels are formed.
- 35 7. (Amended) The wafer prober according to Claim 6, wherein said channels formed on the surface of said ceramic substrate are provided with air suction holes.
8. (Amended) A wafer prober which comprises a ceramic

ABSTRACT

This invention is related to a wafer prober wherein a ceramic substrate is formed with a conductor layer on its surface.

1 / 9

Fig. 1

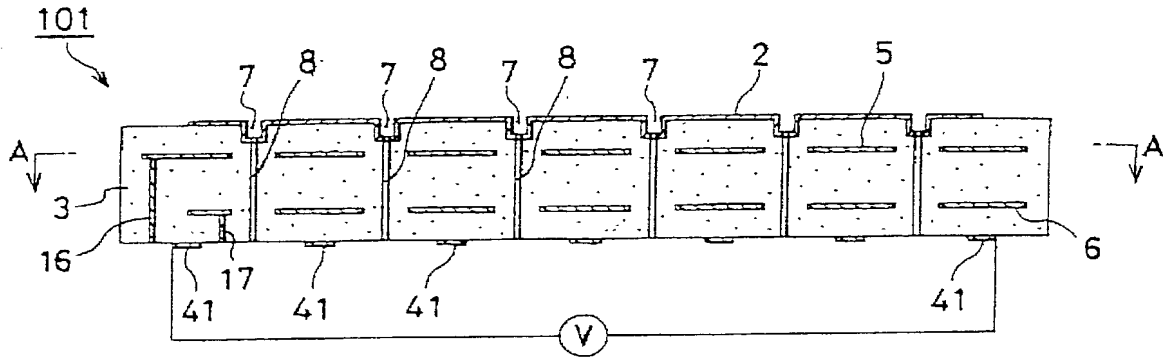


Fig. 2

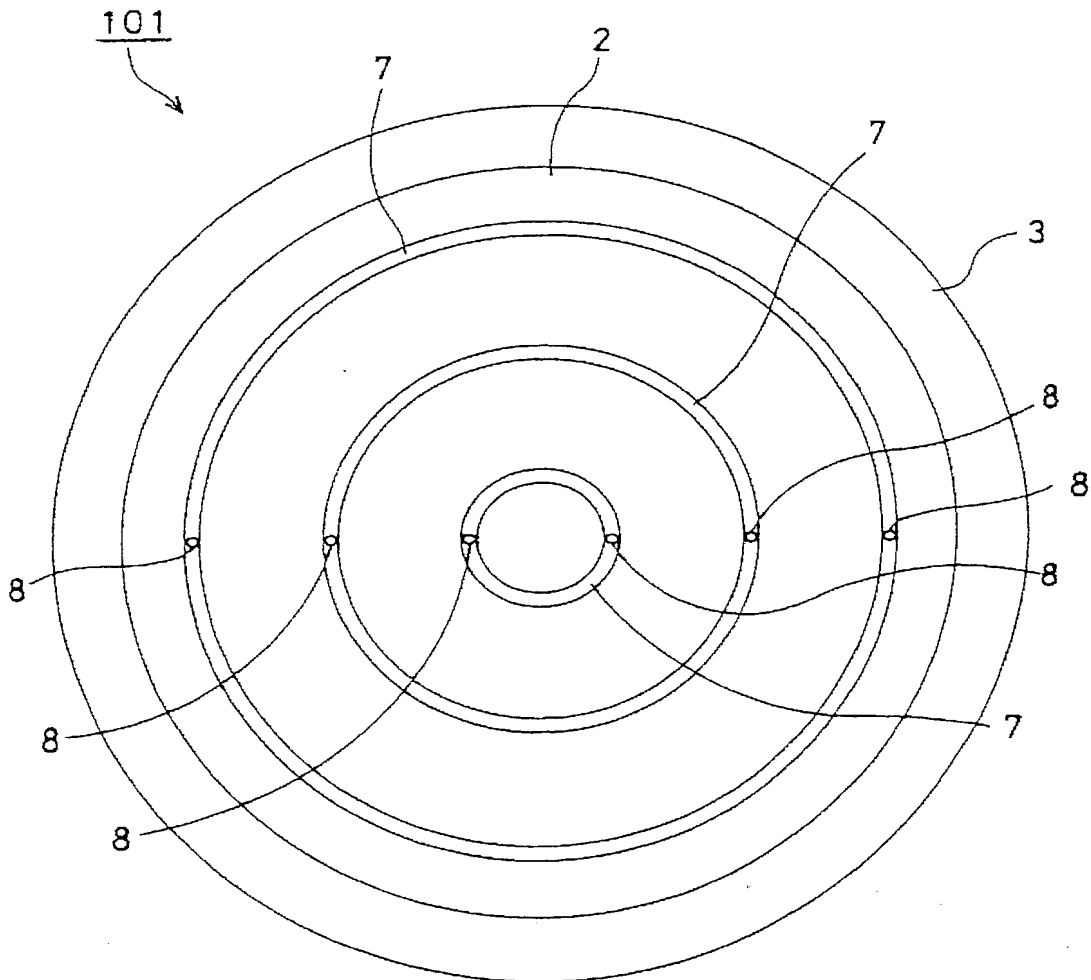


Fig. 3

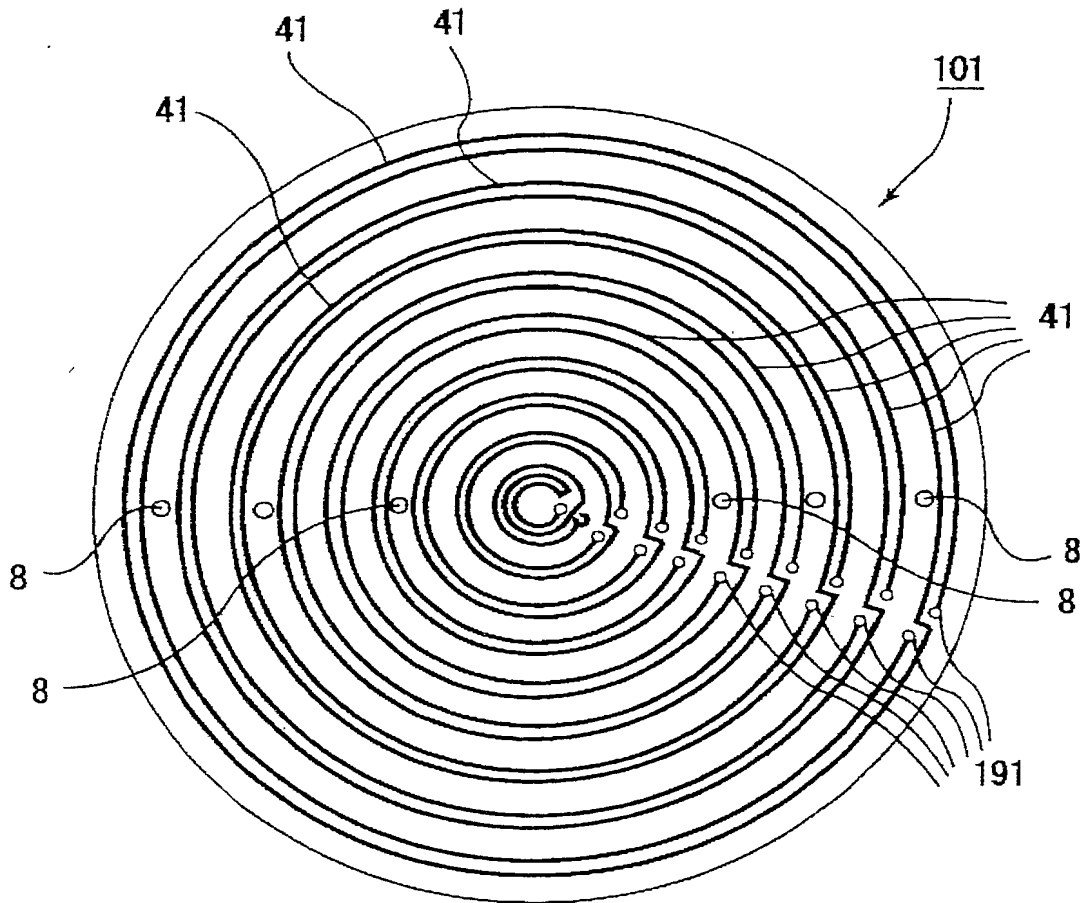


Fig. 4

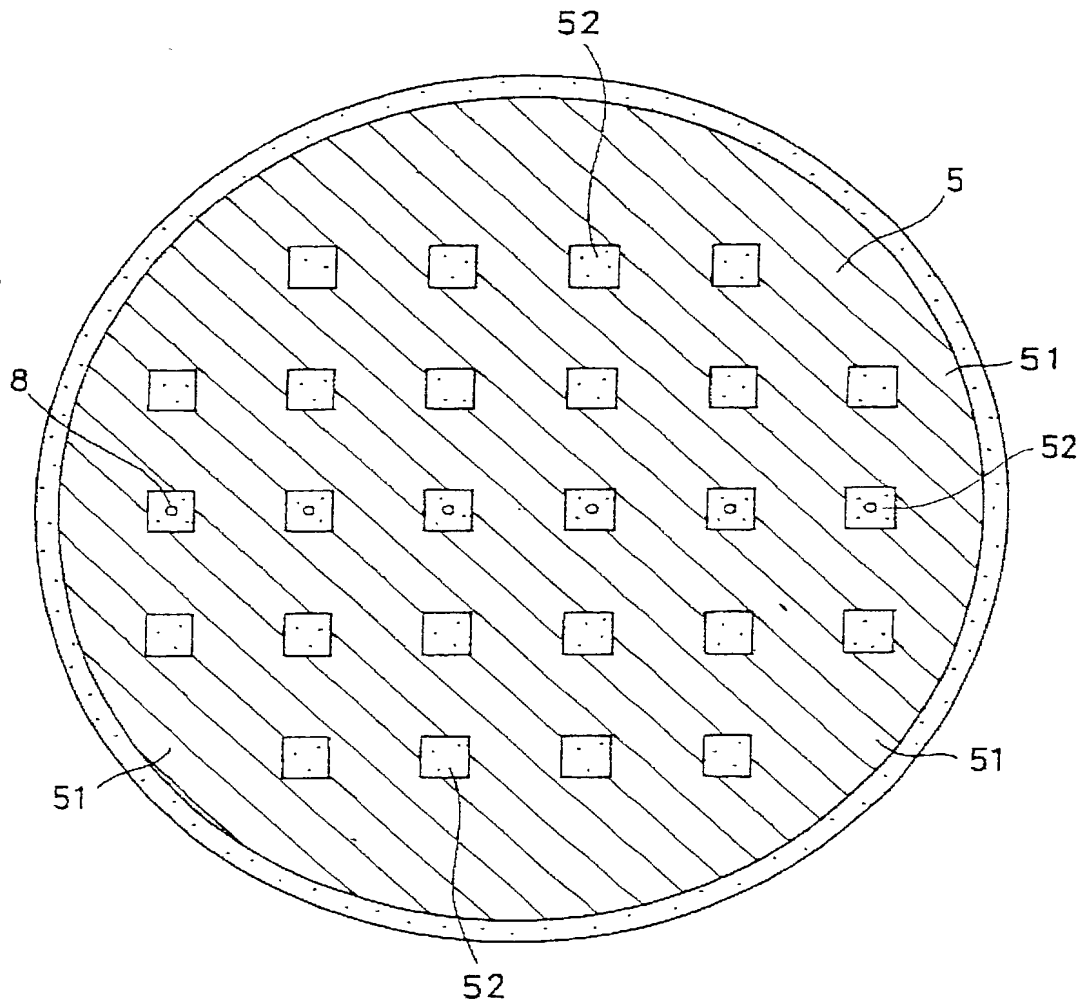


Fig. 5

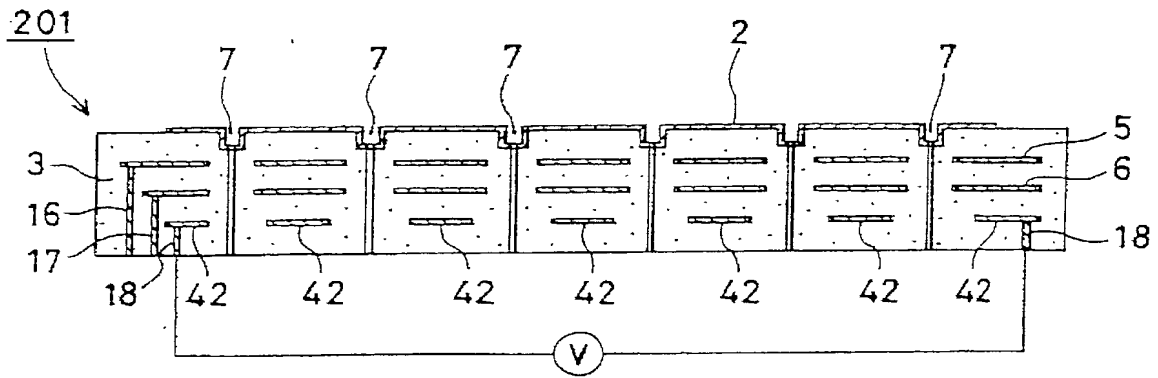


Fig. 6

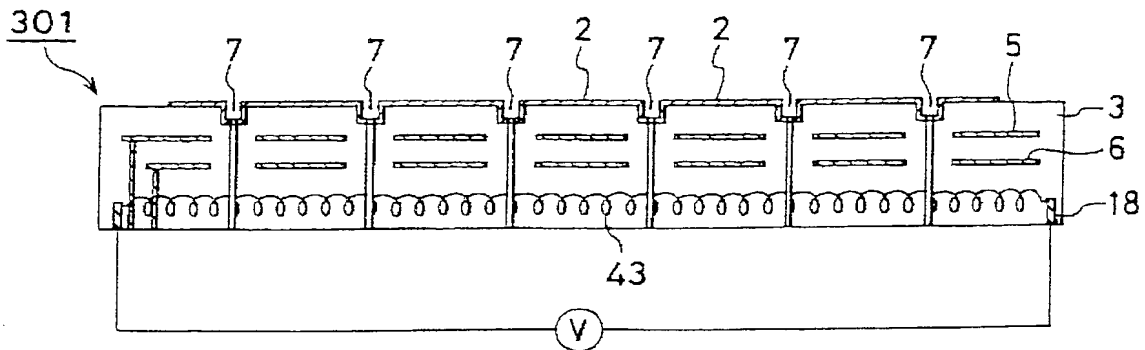


Fig. 7

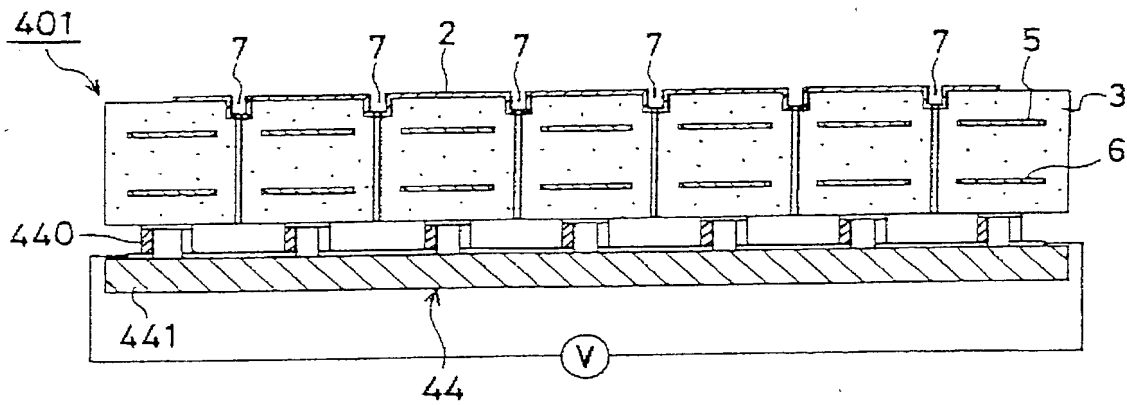


Fig. 8

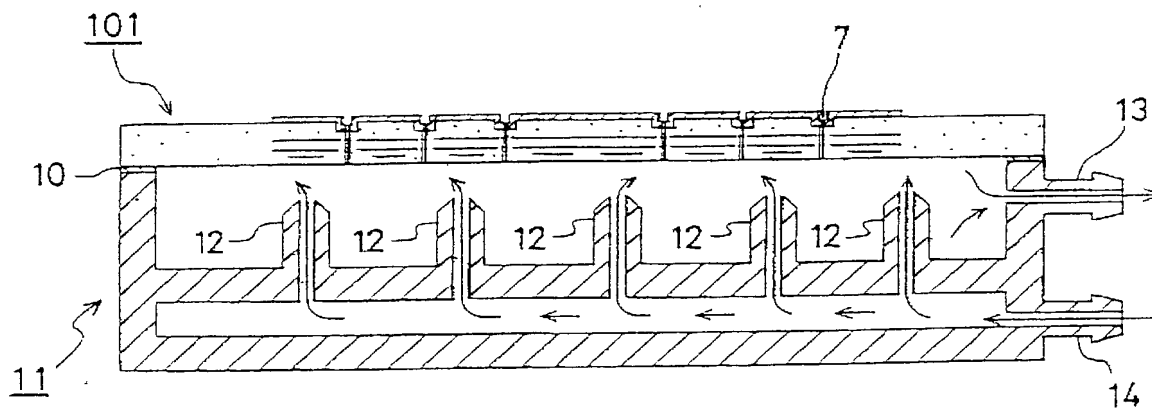


Fig. 9

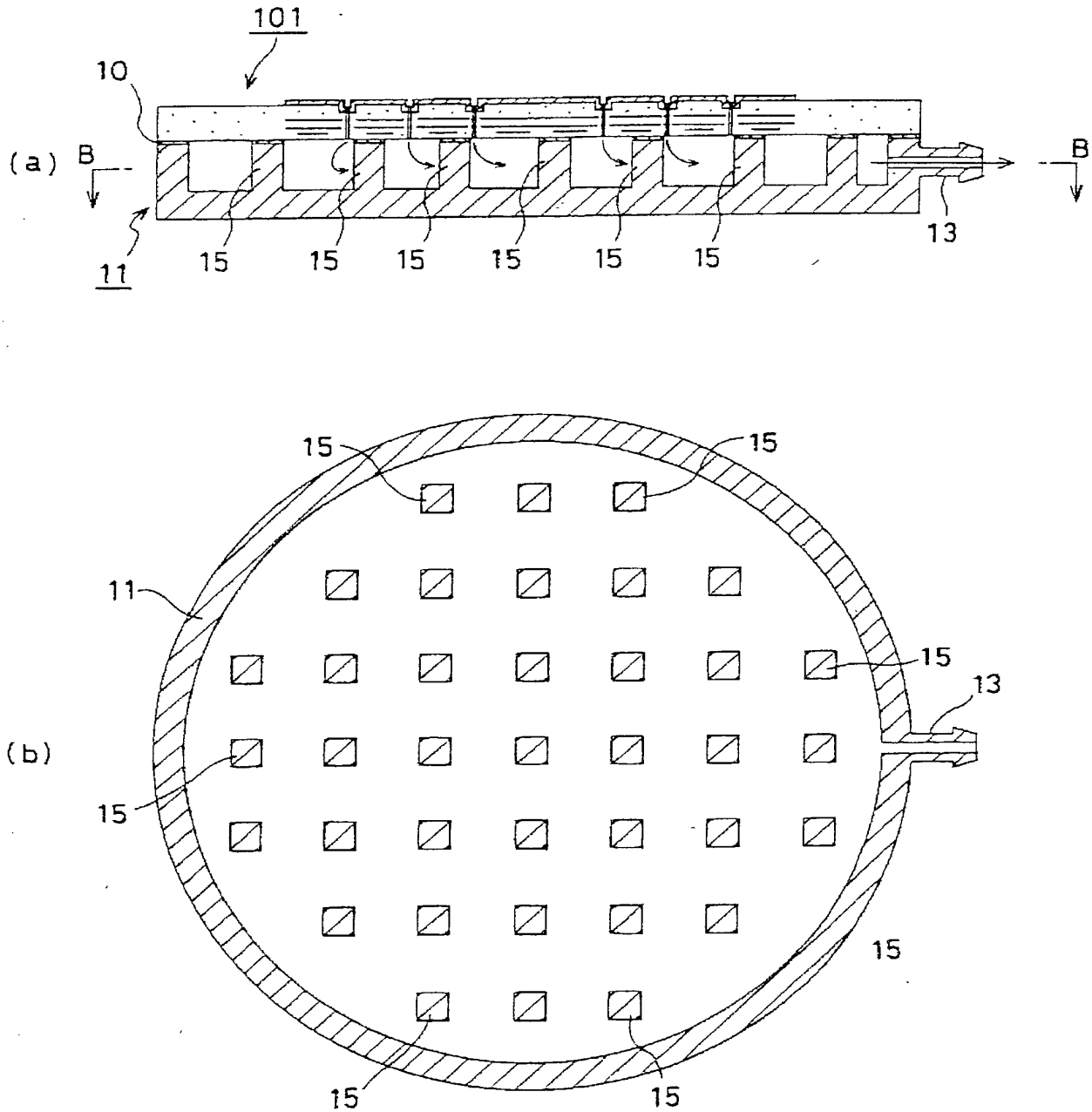


Fig. 10

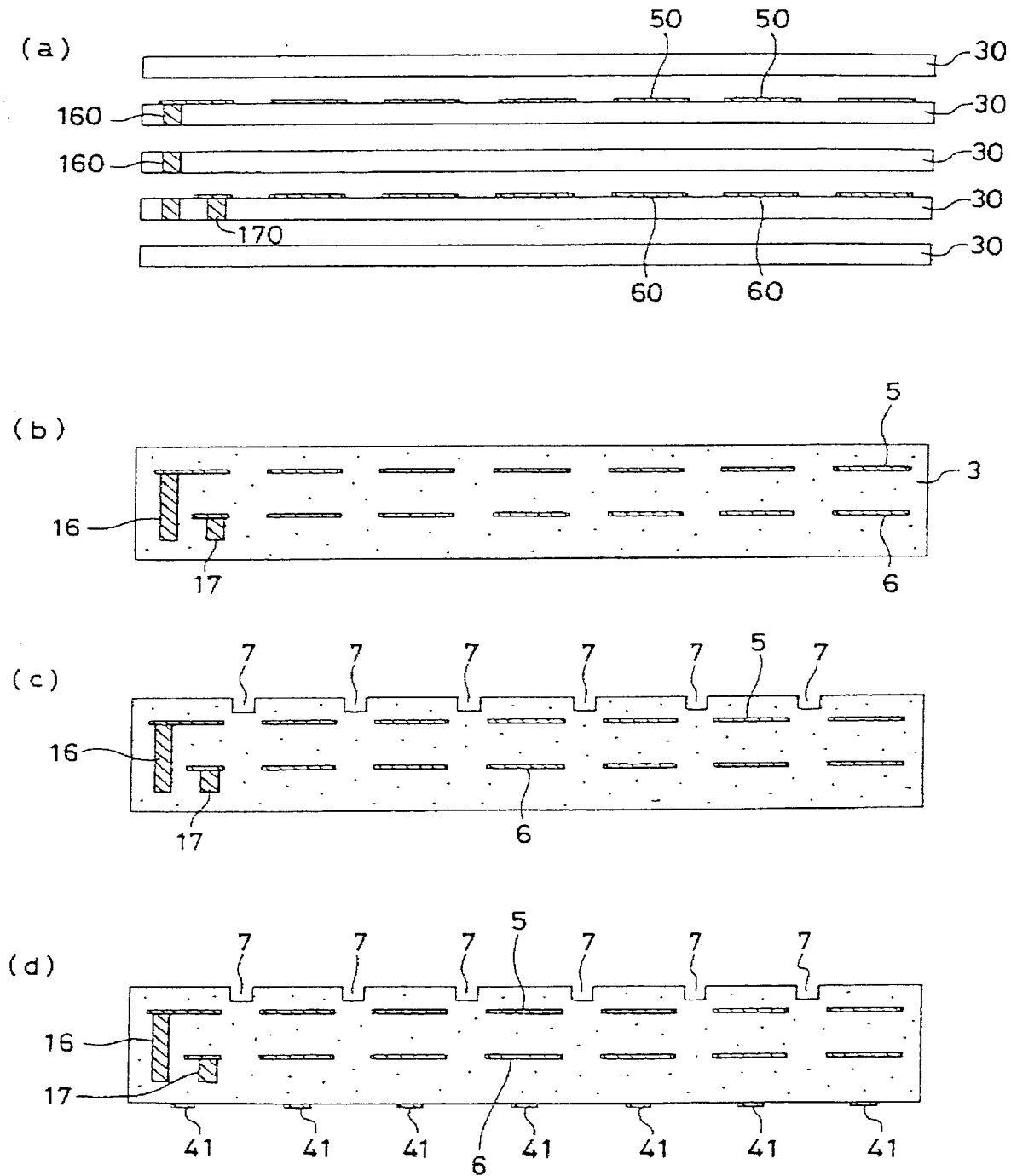


Fig. 11

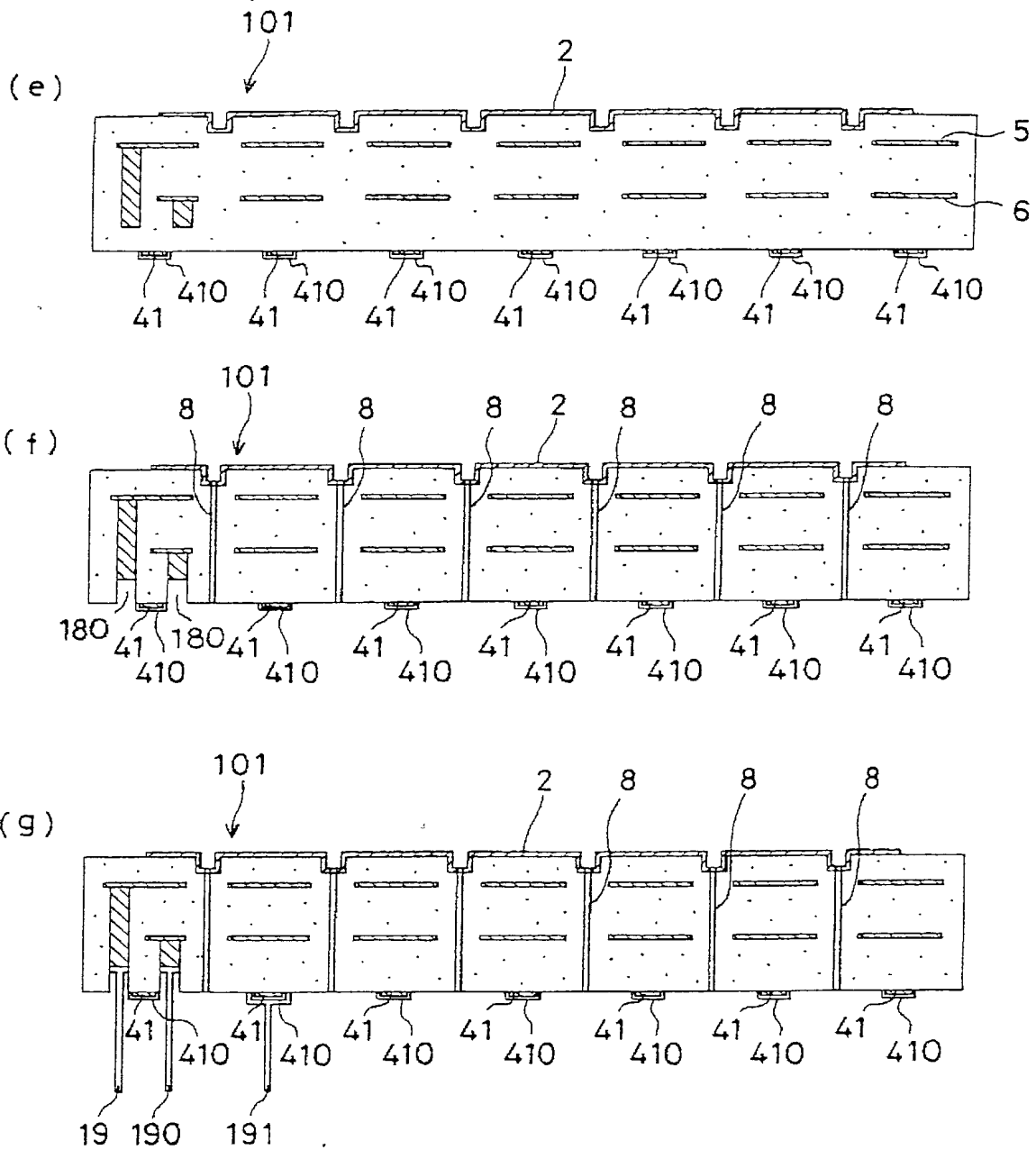


Fig. 12

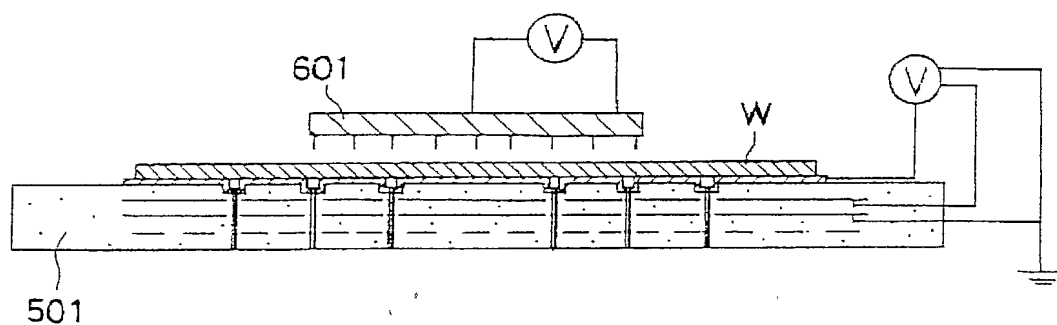
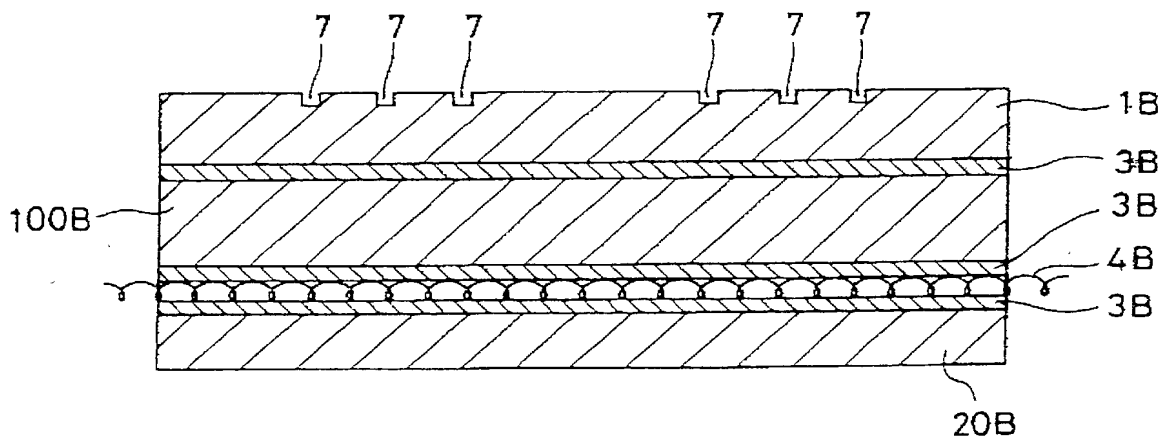


Fig. 13

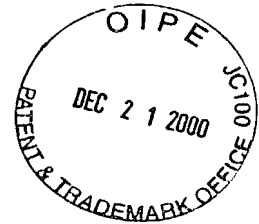


Declaration and Power of Attorney for Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書



下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

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My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

WAFER PROBER

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

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（該当する場合） _____ に訂正されました。

☒ was filed on October 24, 2000
as United States Application Number
09/673,953 (PCT International Application
Number PCT/JP99/05693, amended on
3/21/00) and was amended on
10/24/00 (if applicable)

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

Japanese Language Declaration

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Prior foreign application(s)
外国での先行出願

PCT/JP99/05693
(Number)
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International
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(Filing Date)
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での期間中に入手された、連邦規則法典第37編1条56項
で定義された特許資格の有無に関する重要な情報について開
示義務があることを認識しています。

(Application No.)
(出願番号)

(Filing Date)
(出願日)

(Application No.)
(出願番号)

(Filing Date)
(出願日)

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18編第1001条に基づき、罰金または拘禁、もしくはそ
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く宣誓を致します。

I hereby claim foreign priority under Title 35, United States
Code, § 119(a)-(d) or § 365 (b) of any foreign application(s) for
patent or inventor's certificate, or § 365(a) of any PCT
International application which designated at least one country
other than the United States, listed below and have also
identified below, by checking the box, any foreign application
for patent or inventor's certificate, or PCT International
application having a filing date before that of the application on
which priority is claimed.

Priority Not Claimed
優先権主張なし

October 15, 1999
(Day/Month/Year Filed)
(出願年月日)

(Day/Month/Year Filed)
(出願年月日)

(Day/Month/Year Filed)
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, §
119(e) of any United States provisional application(s) listed
below.

(Application No.)
(出願番号)

(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, §
120 of any United States application(s), or § 365(c) of any PCT
International application designating the United States, listed
below and, insofar as the subject matter of each of the claims of
this application is not disclosed in the prior United States or PCT
International application in the manner provided by the first
paragraph of Title 35, United States Code, § 112, I acknowledge
the duty to disclose information which is material to patentability
as defined in Title 37, Code of Federal Regulations, § 1.56
which became available between the filing date of the prior
application and the national or PCT International filing date of
this application.

(Status)(patented, pending, abandoned)
(現況：特許許可済、係属中、放棄済)

(Status)(patented, pending, abandoned)
(現況：特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own
knowledge are true and that all statements made on information
and belief are believed to be true; and further that these
statements were made with the knowledge that willful false
statements and the like so made are punishable by fine or
imprisonment, or both, under Section 1001 of Title 18 of the
United States Code and that such willful false statements may
jeopardize the validity of the application or any patent issued
thereon.

Japanese Language Declaration

日本語宣言

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁理士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (list name and registration number)

John H. Mion, Reg. No. 18,879; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; Brett S. Sylvester, Reg. No. 32,765; Robert M. Masters, Reg. No. 35,603; George F. Lehnigk, Reg. No. 36,359; John T. Callahan, Reg. No. 32,607 and Steven M. Gruskin, Reg. No. 36,818.

書類送付先

Send Correspondence to:
SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W. Suite 800
Washington, D.C. 20037-3213

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to:

(202)293-7060

唯一または第一発明者名	1-00	Full name of sole or first inventor Atsushi ITO
発明者の署名	日付	Inventor's signature Atsushi Ito
住所		Residence Gifu, Japan JPX
国籍		Citizenship Japanese
私書箱		Post Office Address C/o IBIDEN CO., LTD. 1-1, Kitagata, Ibigawacho, Ibi-gun, Gifu 501-0695, Japan
第二共同発明者	2-00	Full name of second joint inventor, if any Yasuji HIRAMATSU
第二共同発明者	日付	Second inventor's signature Yasuji Hiramatsu
住所		Residence Gifu, Japan JPX
国籍		Citizenship Japanese
私書箱		Post Office Address C/o IBIDEN CO., LTD. 1-1, Kitagata, Ibigawacho, Ibi-gun, Gifu 501-0695, Japan

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration

日本語宣言

第三の共同発明者の氏名 (該当する場合)	3-00	Full name of third joint inventor, if any Yasutaka ITO
同第三発明者の署名	日付	Third inventor's signature Yasutaka Ito DEC. 14. 2000
住所		Residence Gifu, Japan JPX
国籍		Citizenship Japanese
郵便の宛先		Post office address C/o IBIDEN CO., LTD. 1-1, Kitagata, Ibigawacho, Ibi-gun, Gifu 501-0695, Japan
第四の共同発明者の氏名 (該当する場合)	4-00	Full name of fourth joint inventor, if any Masakazu FURUKAWA
同第四発明者の署名	日付	Fourth inventor's signature Masakazu Furukawa DEC. 14. 2000
住所		Residence Gifu, Japan JPX
国籍		Citizenship Japanese
郵便の宛先		Post office address C/o IBIDEN CO., LTD. 1-1, Kitagata, Ibigawacho, Ibi-gun, Gifu 501-0695, Japan
第五の共同発明者の氏名 (該当する場合)		
同第五発明者の署名	日付	Full name of fifth joint inventor, if any
住所		Fifth inventor's signature Date
国籍		Residence
郵便の宛先		Citizenship
		Post office address
第六の共同発明者の氏名 (該当する場合)		
同第六発明者の署名	日付	Full name of sixth joint inventor, if any
住所		Sixth inventor's signature Date
国籍		Residence
郵便の宛先		Citizenship
		Post office address